FIG.1 (PRIOR ART)

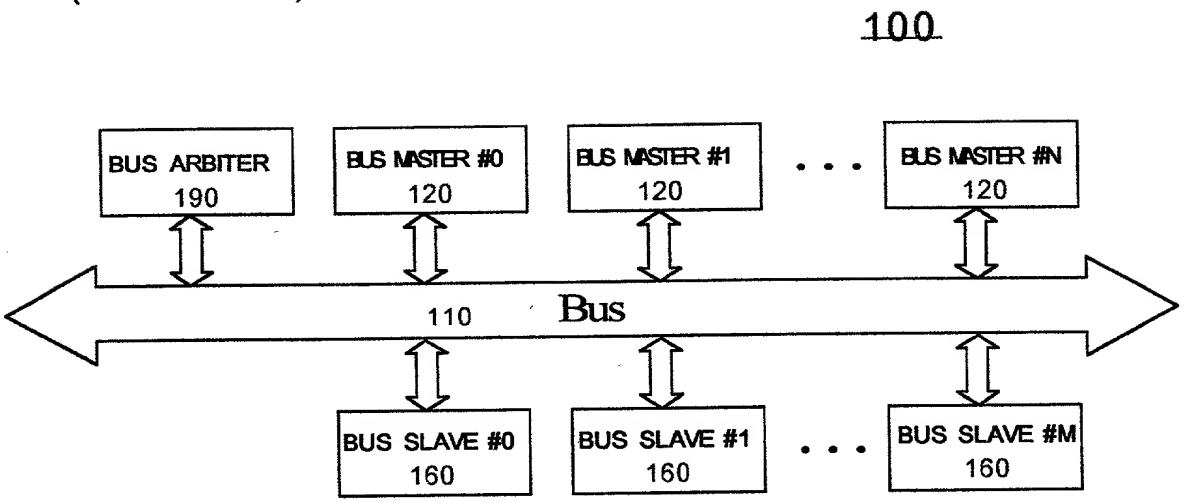

FIG.2 (PRIOR ART)

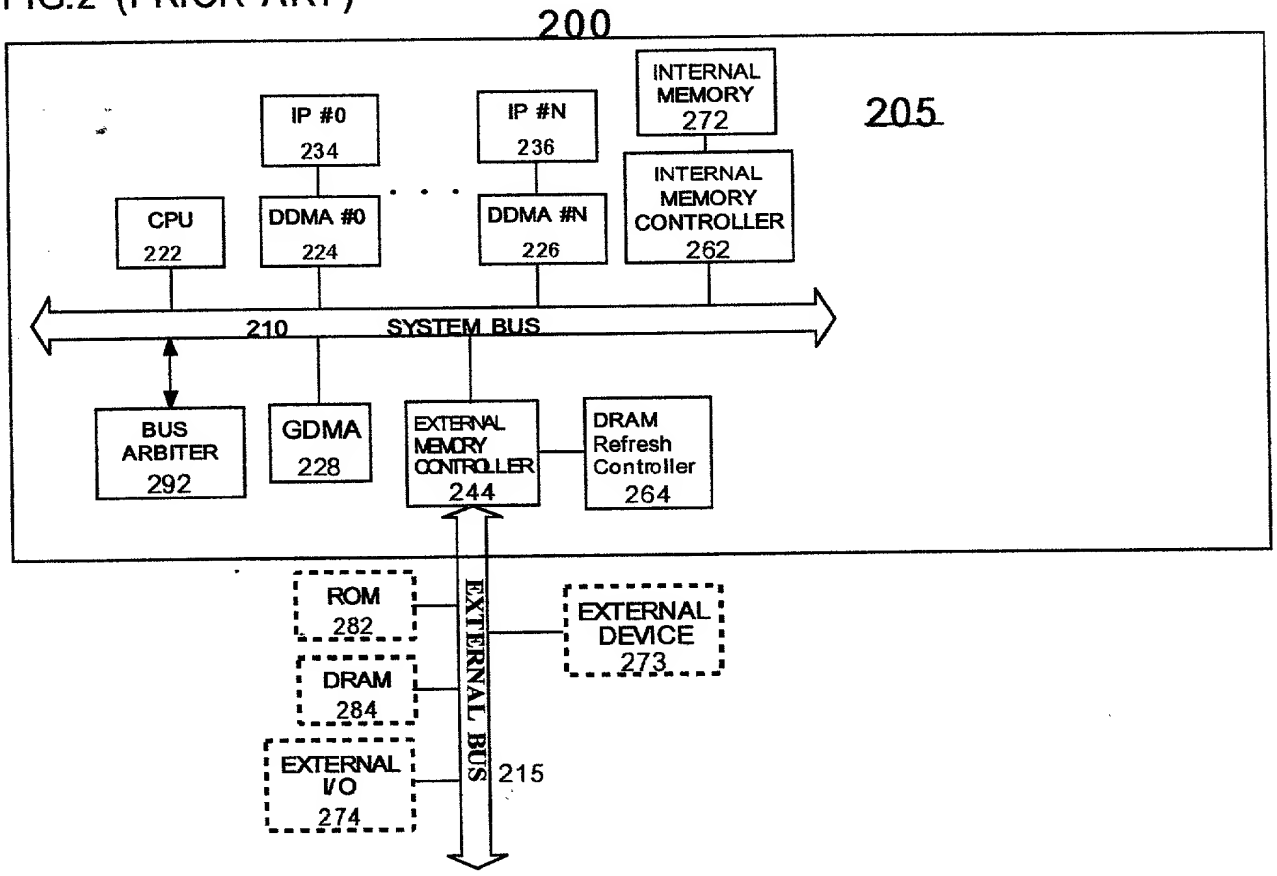

FIG.2B (PRIOR ART)

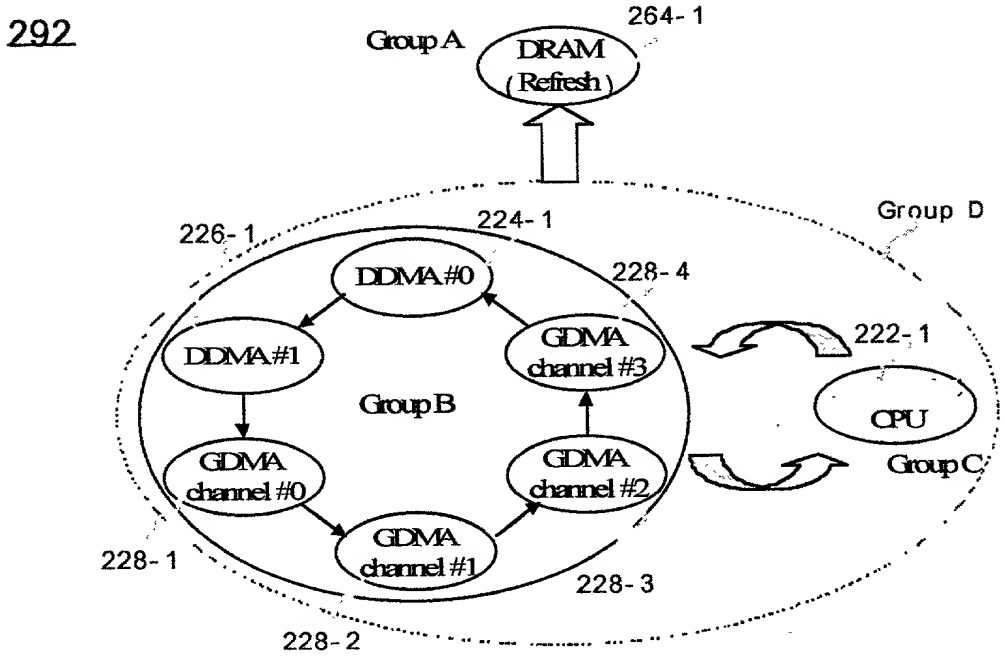

FIG.2C (PRIOR ART)

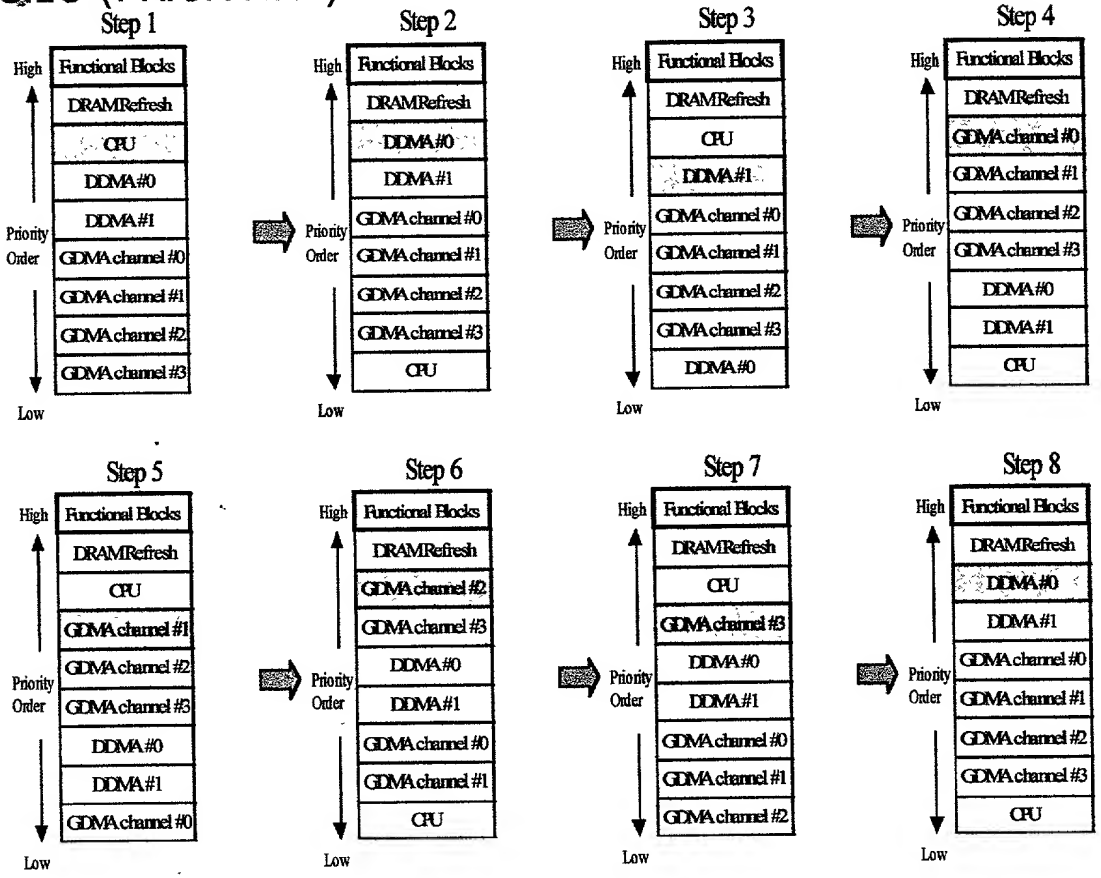

FIG.3A (PRIOR ART)

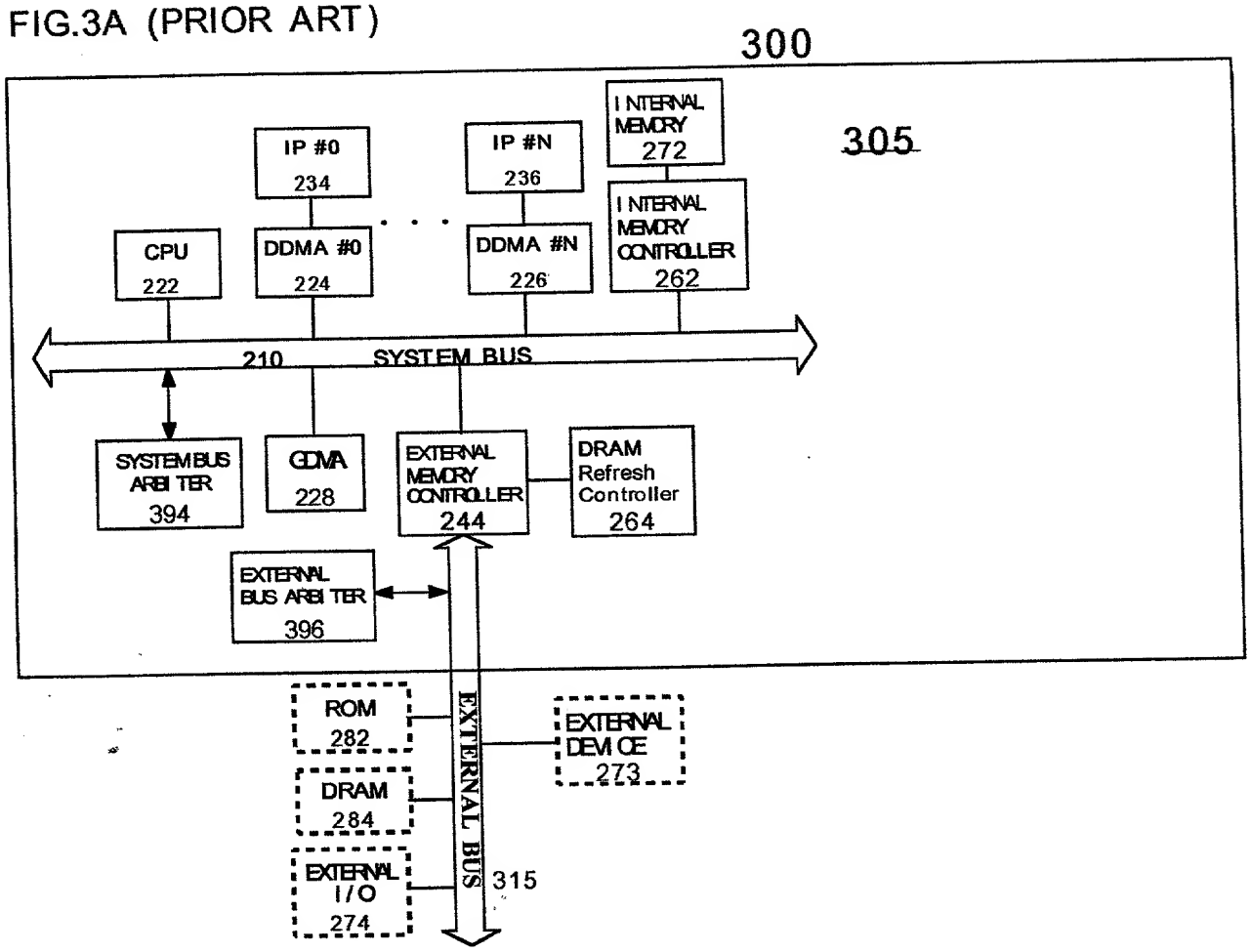

FIG.3B (PRIOR ART)

394

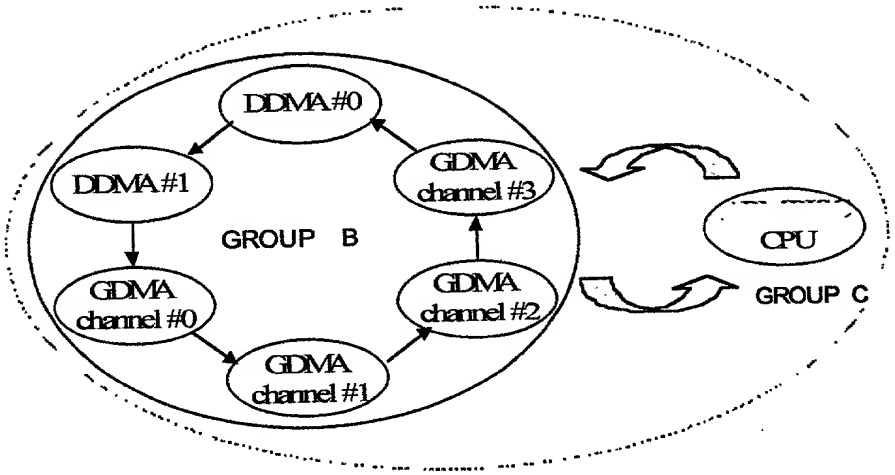

FIG.3C (PRIOR ART)

396

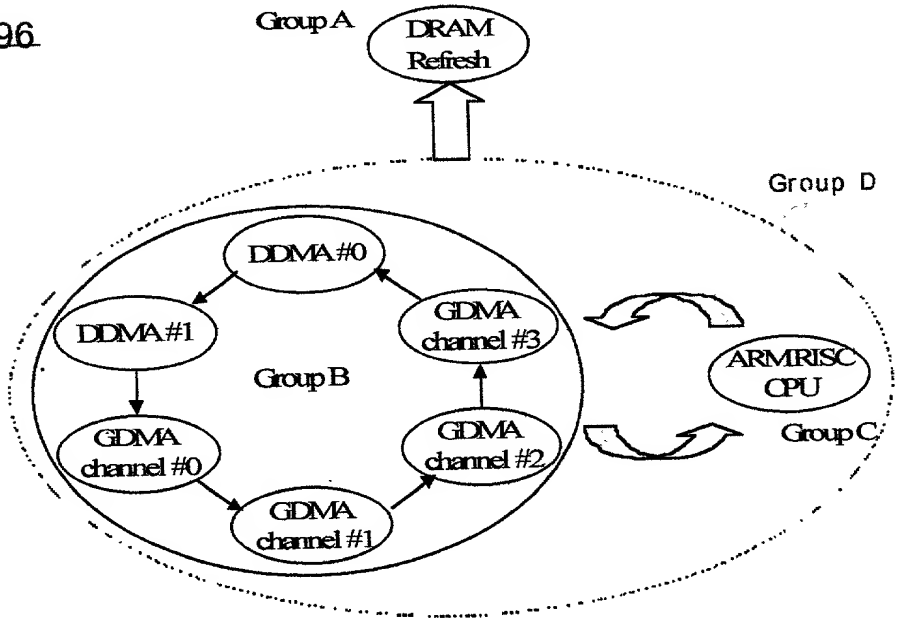

FIG.3D (PRIOR ART)

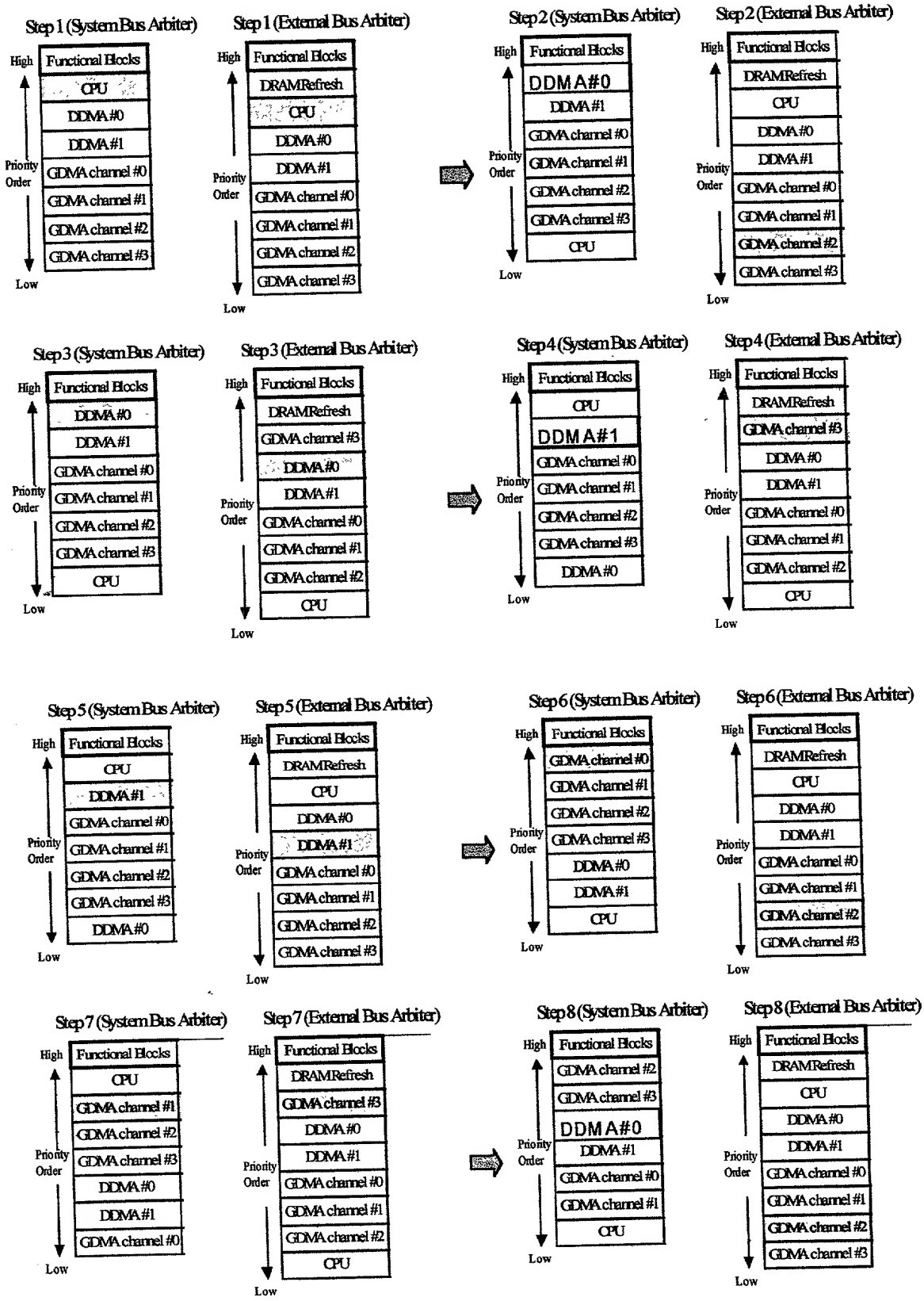

FIG.4

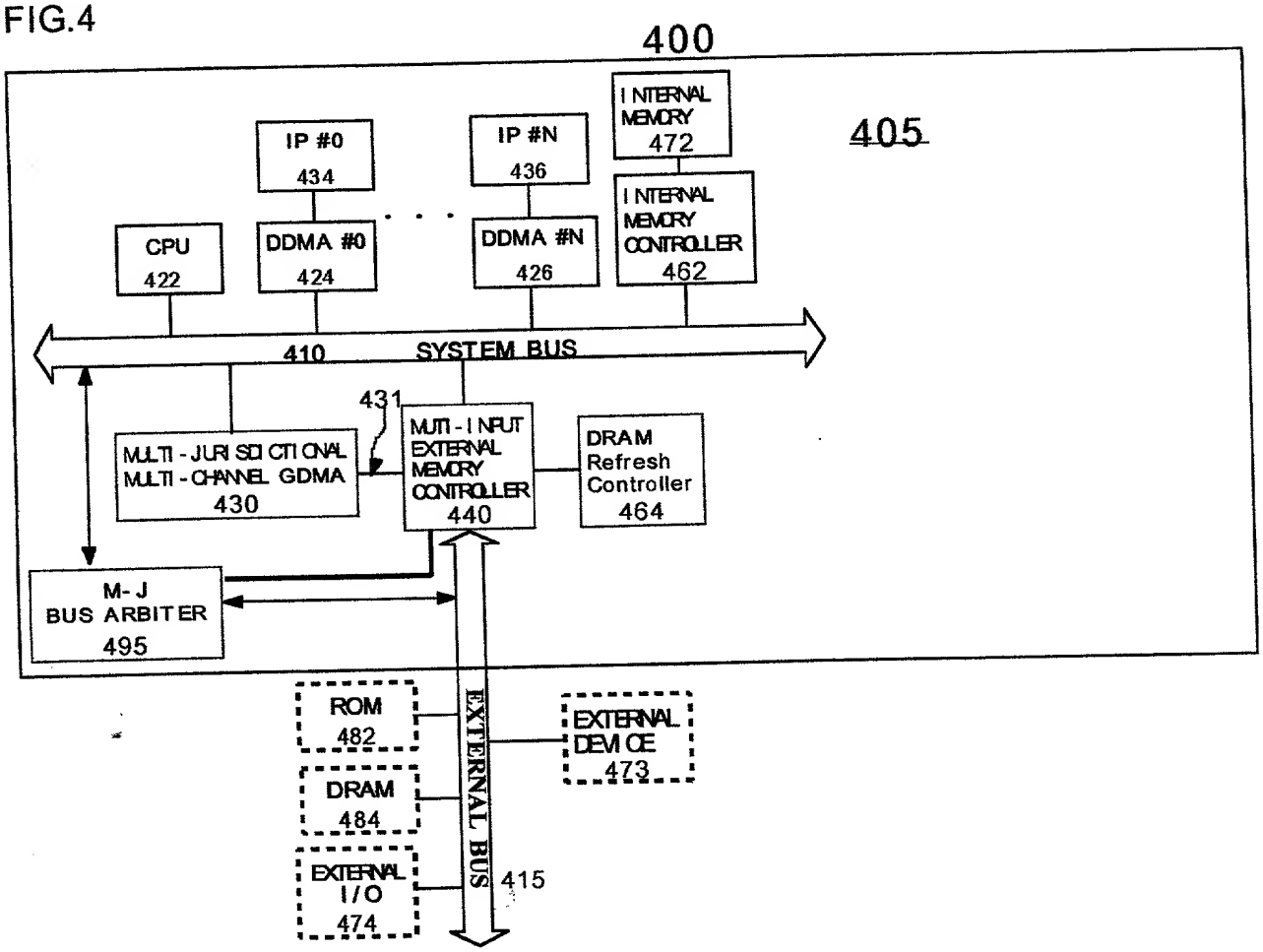
400
405
IP #0
434
IP #N
436
INTERNAL MEMORY
472
INTERNAL MEMORY CONTROLLER
462
CPU
422
DDMA #0
424
DDMA #N
426
410 SYSTEM BUS
431
MULTI-JURISDICTIONAL MULTI-CHANNEL GDMA
430
MUTI-INPUT EXTERNAL MEMORY CONTROLLER
440
DRAM Refresh Controller
464
M-J BUS ARBITER
495
ROM
482
DRAM
484
EXTERNAL I/O
474
EXTERNAL BUS
415
EXTERNAL DEVICE
473

FIG.5

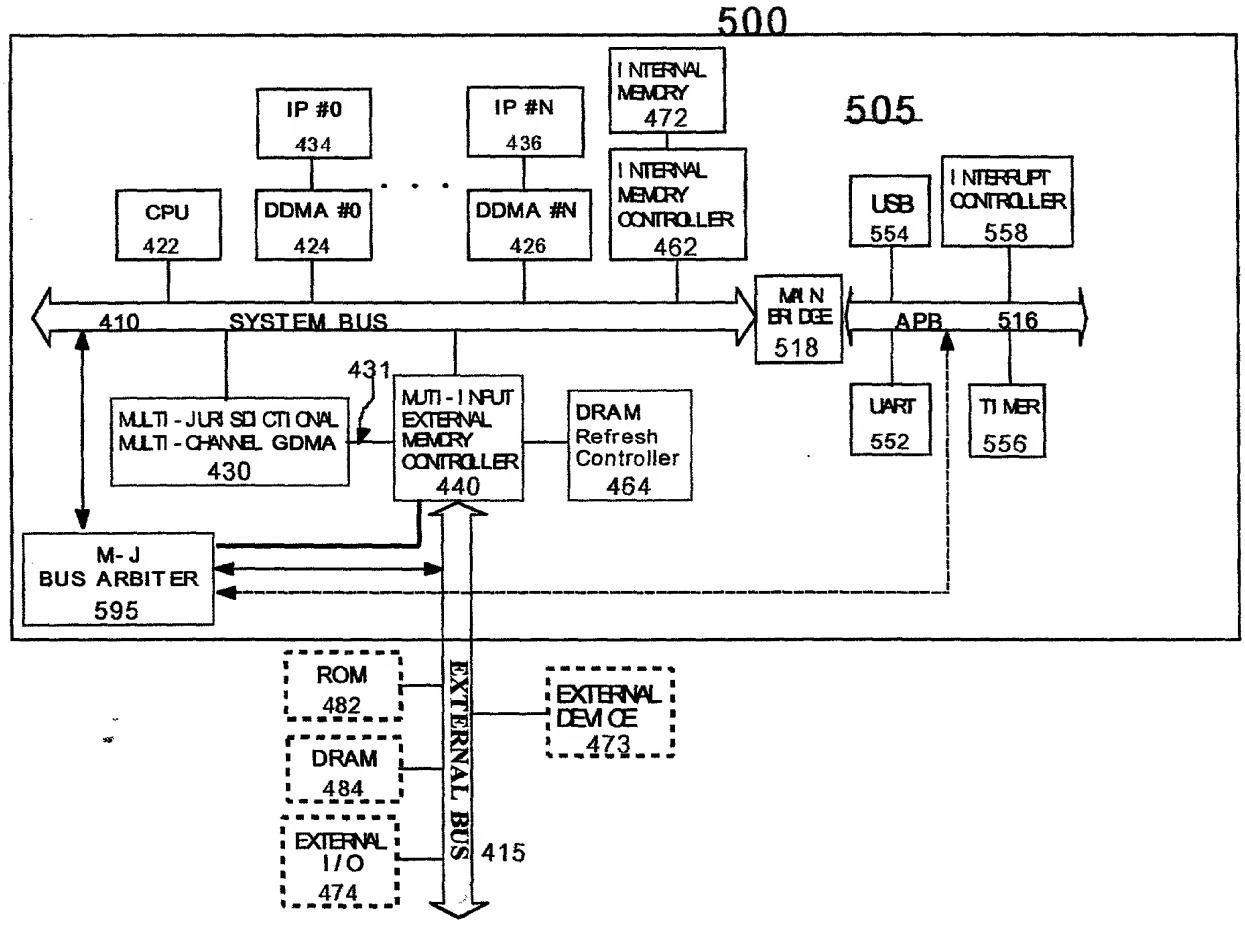
500
505
IP #0
434
IP #N
436
INTERNAL MEMORY
472
INTERNAL MEMORY CONTROLLER
462
CPU
422
DDMA #0
424
DDMA #N
426
USB
554
INTERRUPT CONTROLLER
558
410
SYSTEM BUS
MAIN BRIDGE
518
APB
516
431
MULTI-JURISDICTIONAL MULTI-CHANNEL GDMA
430
MUTI-INPUT EXTERNAL MEMORY CONTROLLER
440
DRAM Refresh Controller
464
UART
552
TIMER
556
M-J BUS ARBITER
595
ROM
482
DRAM
484
EXTERNAL I/O
474
EXTERNAL BUS
415
EXTERNAL DEVICE
473

FIG.6

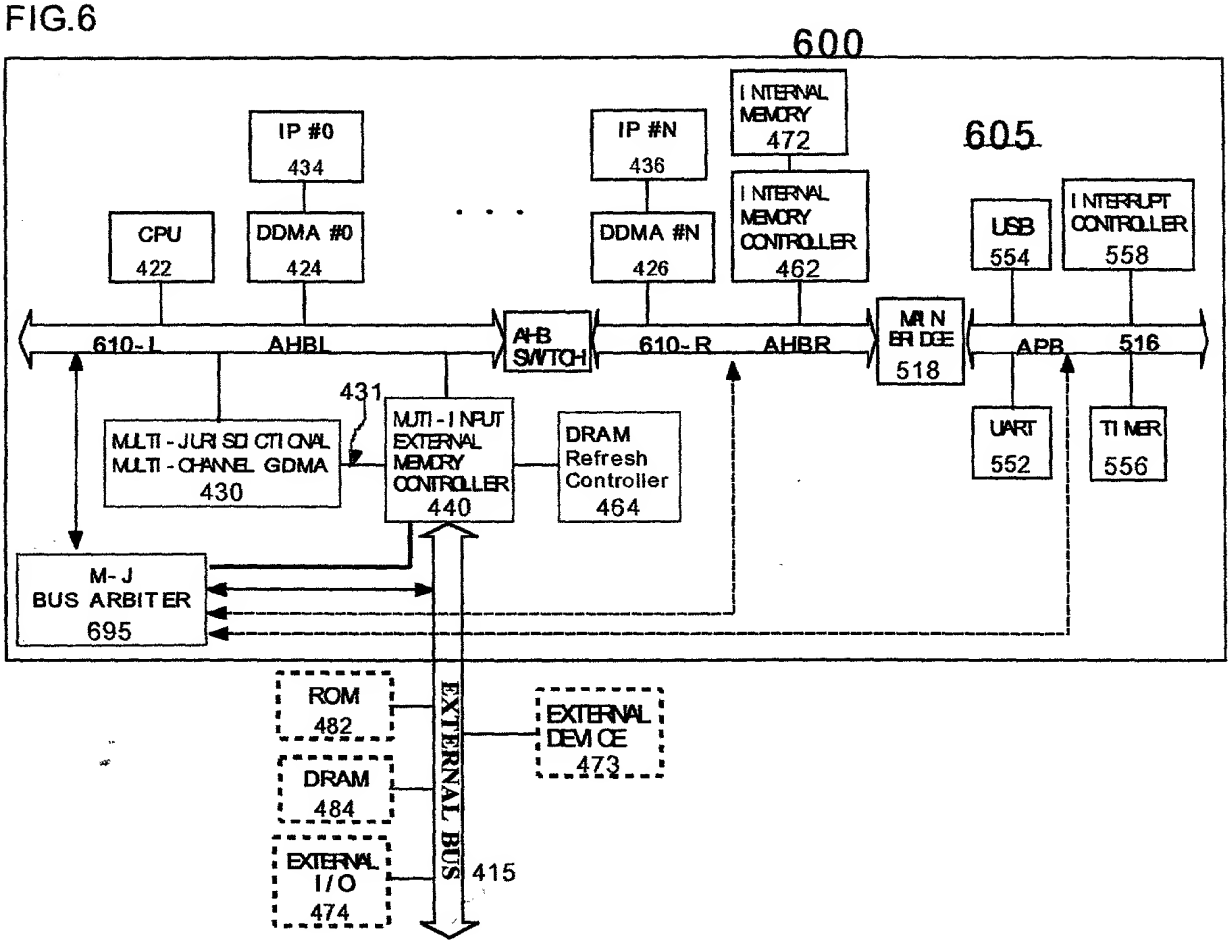
600
IP #0
434
IP #N
436
INTERNAL MEMORY
472
605
CPU
422
DDMA #0
424
DDMA #N
426
INTERNAL MEMORY CONTROLLER
462
USB
554
INTERRUPT CONTROLLER
558
610-L
AHBL
AHB SWITCH
610-R
AHBR
MAIN BRIDGE
518
APB
516
431
MULTI-JURISDICTIONAL MULTI-CHANNEL GDMA
430
MULTI-INPUT EXTERNAL MEMORY CONTROLLER
440
DRAM Refresh Controller
464
UART
552
TIMER
556
M-J BUS ARBITER
695
ROM
482
DRAM
484
EXTERNAL I/O
474
EXTERNAL DEVICE
473
EXTERNAL BUS
415

FIG.7

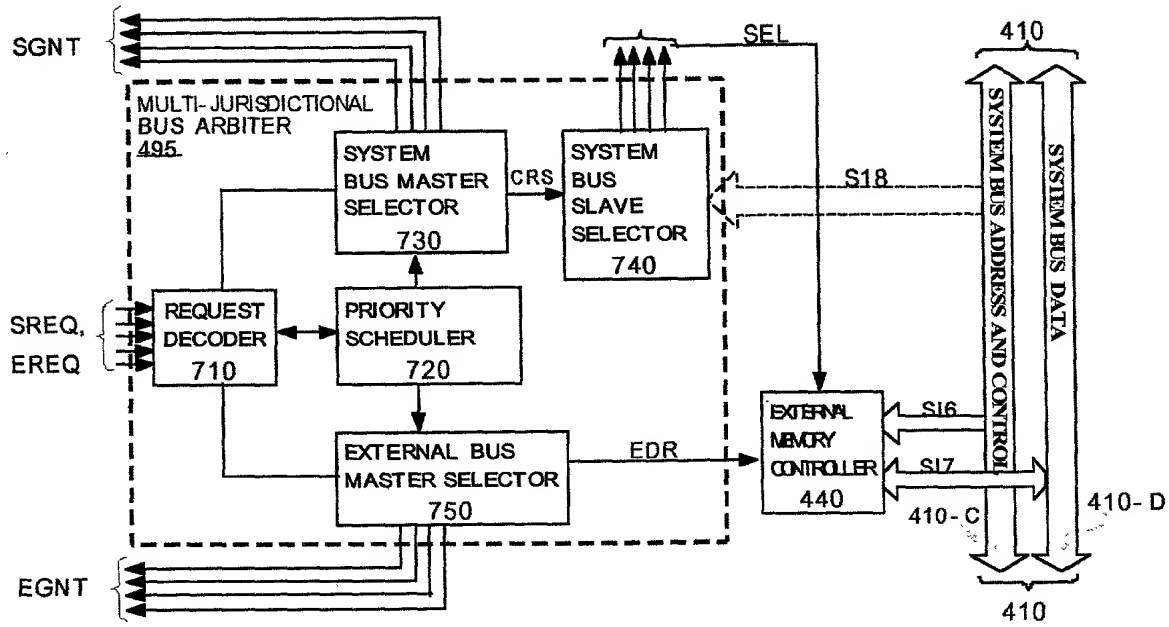
SGNT
MULTI-JURISDICTIONAL BUS ARBITER 495
SYSTEM BUS MASTER SELECTOR 730
CRS
SYSTEM BUS SLAVE SELECTOR 740
SEL
410
SYSTEM BUS ADDRESS AND CONTROL
SYSTEM BUS DATA
S18
SREQ, EREQ
REQUEST DECODER 710
PRIORITY SCHEDULER 720
EXTERNAL BUS MASTER SELECTOR 750
EDR
EXTERNAL MEMORY CONTROLLER 440
S16
S17
410-C
410-D
EGNT
410

FIG.8

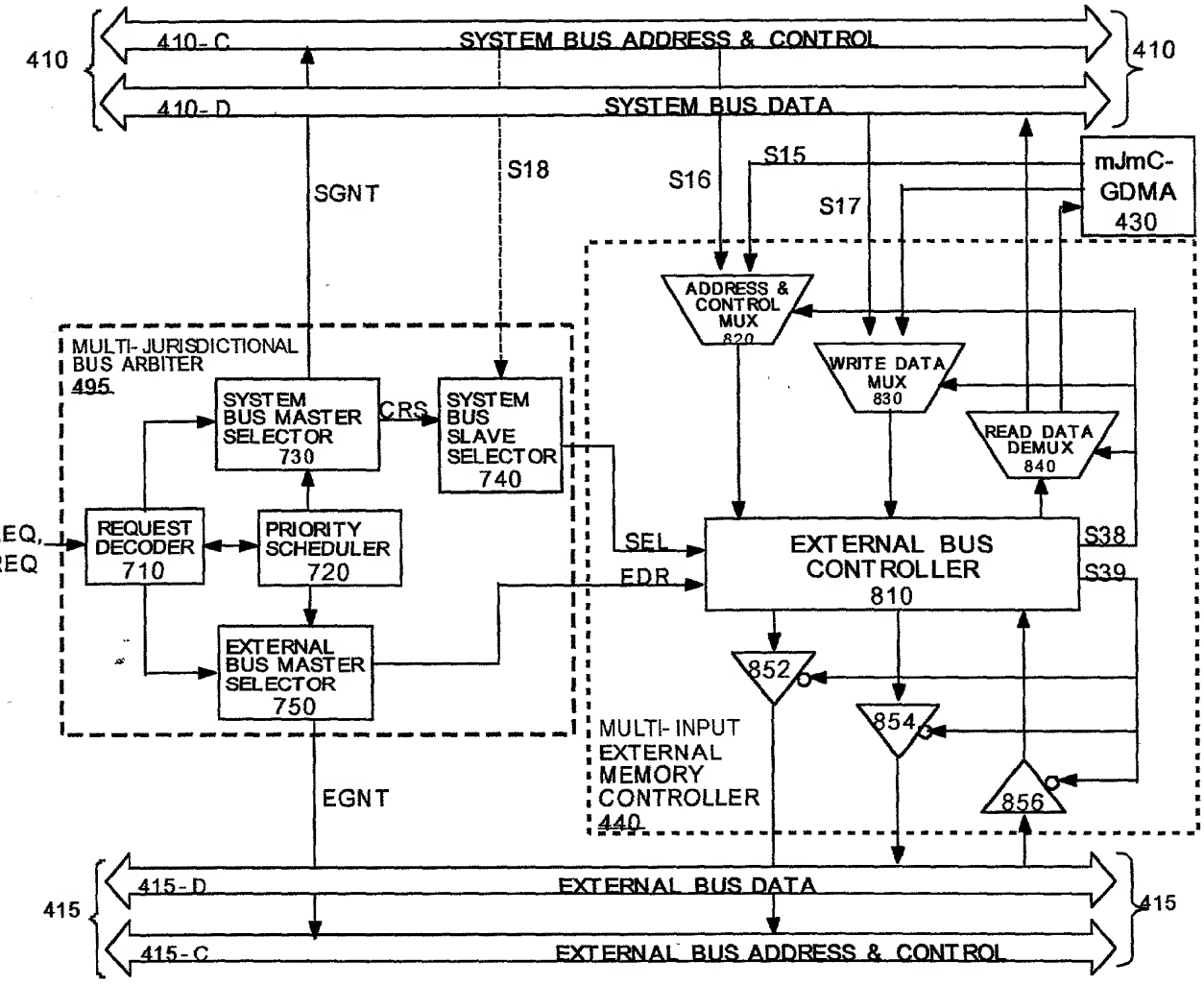
410
410-C
SYSTEM BUS ADDRESS & CONTROL
410
410-D
SYSTEM BUS DATA
SGNT
S18
S16
S15
S17
mJmC-GDMA 430
ADDRESS & CONTROL MUX 820
WRITE DATA MUX 830
READ DATA DEMUX 840
MULTI-JURISDICTIONAL BUS ARBITER 495
SYSTEM BUS MASTER SELECTOR 730
CRS
SYSTEM BUS SLAVE SELECTOR 740
SREQ, EREQ
REQUEST DECODER 710
PRIORITY SCHEDULER 720
SEL
EDR
EXTERNAL BUS CONTROLLER 810
S38
S39
EXTERNAL BUS MASTER SELECTOR 750
852
854
856
MULTI-INPUT EXTERNAL MEMORY CONTROLLER 440
EGNT
415
415-D
EXTERNAL BUS DATA
415
415-C
EXTERNAL BUS ADDRESS & CONTROL

FIG.9

		External bus master	System bus master	
	No request REQ[1:0] = 2'b00	External bus only REQ[1:0] = 2'b10	System bus only REQ[1:0] = 2'b01	Both buses REQ[1:0] = 2'b11
DRAM refresh controller	O	O	X	X
CPU	O	X	O	O
DDMA block	O	X	O	O
GDMA channel	O	O	O	O
External device	O	O	X	X

FIG.11

Classification of set	Element
Set of functional blocks making a system bus request (system bus master, S)	CPU, DDMA block, and GDMA block
Set of functional blocks making an external bus request (E)	DRAM refresh controller, CPU, DDMA block, GDMA channel, and external device
Set of functional blocks making only a system bus request (SO)	CPU
Set of functional blocks making only an external bus request (EO)	DRAM refresh controller, GDMA channel, and external device
Set of functional blocks making a request for both system bus and external bus (ES)	CPU, DDMA block, and GDMA channel
Set of functional blocks making requests for a system bus or an external bus (A)	DRAM refresh controller, CPU, DDMA block, GDMA channel, and external device

FIG.10

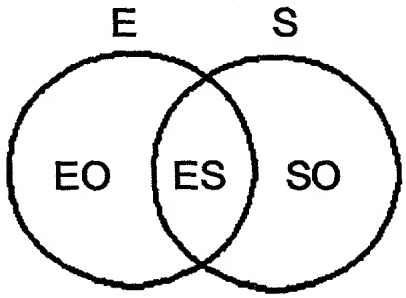

FIG.12

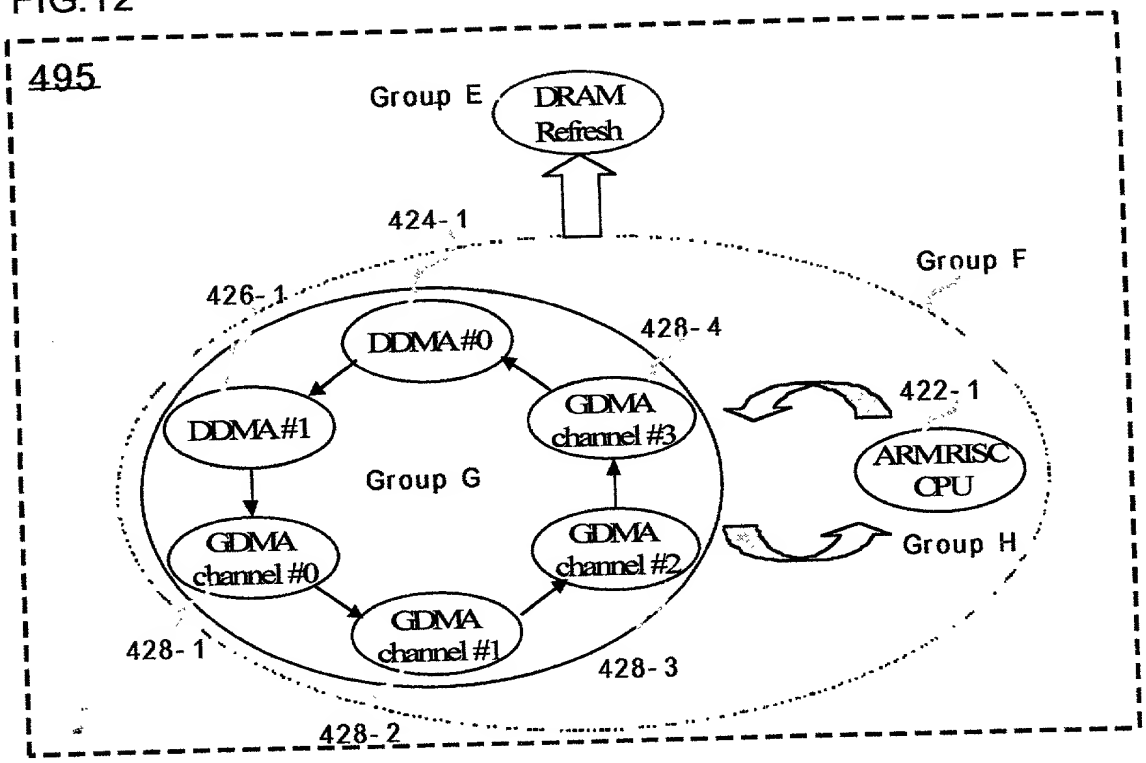
495
Group E
DRAM Refresh
424-1
Group F
426-1
428-4
DDMA#0
DDMA#1
GDMA channel #3
422-1
ARMRISC CPU
Group G
GDMA channel #0
GDMA channel #2
Group H
GDMA channel #1
428-1
428-3
428-2

FIG.13

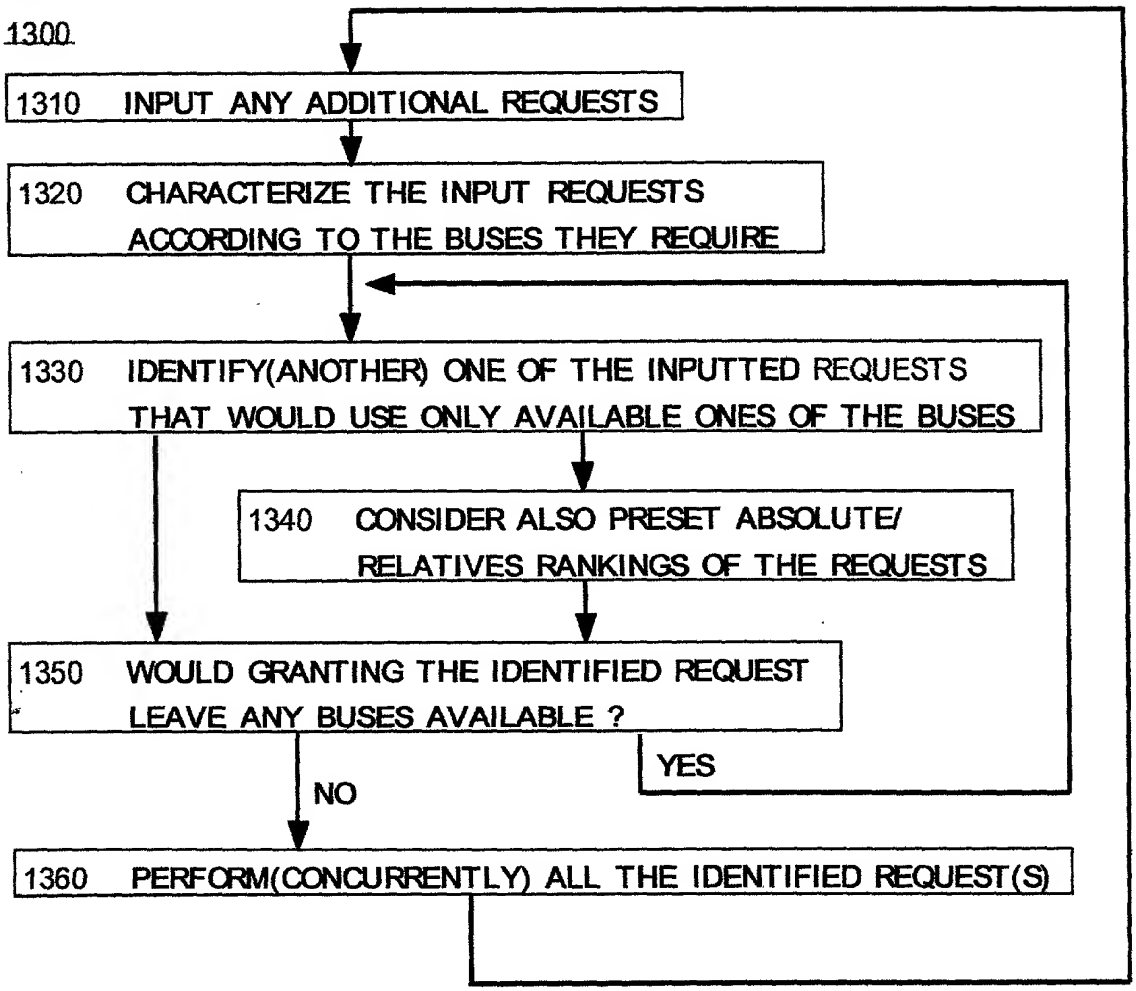
1300
1310 INPUT ANY ADDITIONAL REQUESTS
1320 CHARACTERIZE THE INPUT REQUESTS ACCORDING TO THE BUSES THEY REQUIRE
1330 IDENTIFY(ANOTHER) ONE OF THE INPUTTED REQUESTS THAT WOULD USE ONLY AVAILABLE ONES OF THE BUSES
1340 CONSIDER ALSO PRESET ABSOLUTE/ RELATIVES RANKINGS OF THE REQUESTS
1350 WOULD GRANTING THE IDENTIFIED REQUEST LEAVE ANY BUSES AVAILABLE ?
YES
NO
1360 PERFORM(CONCURRENTLY) ALL THE IDENTIFIED REQUEST(S)

FIG.14

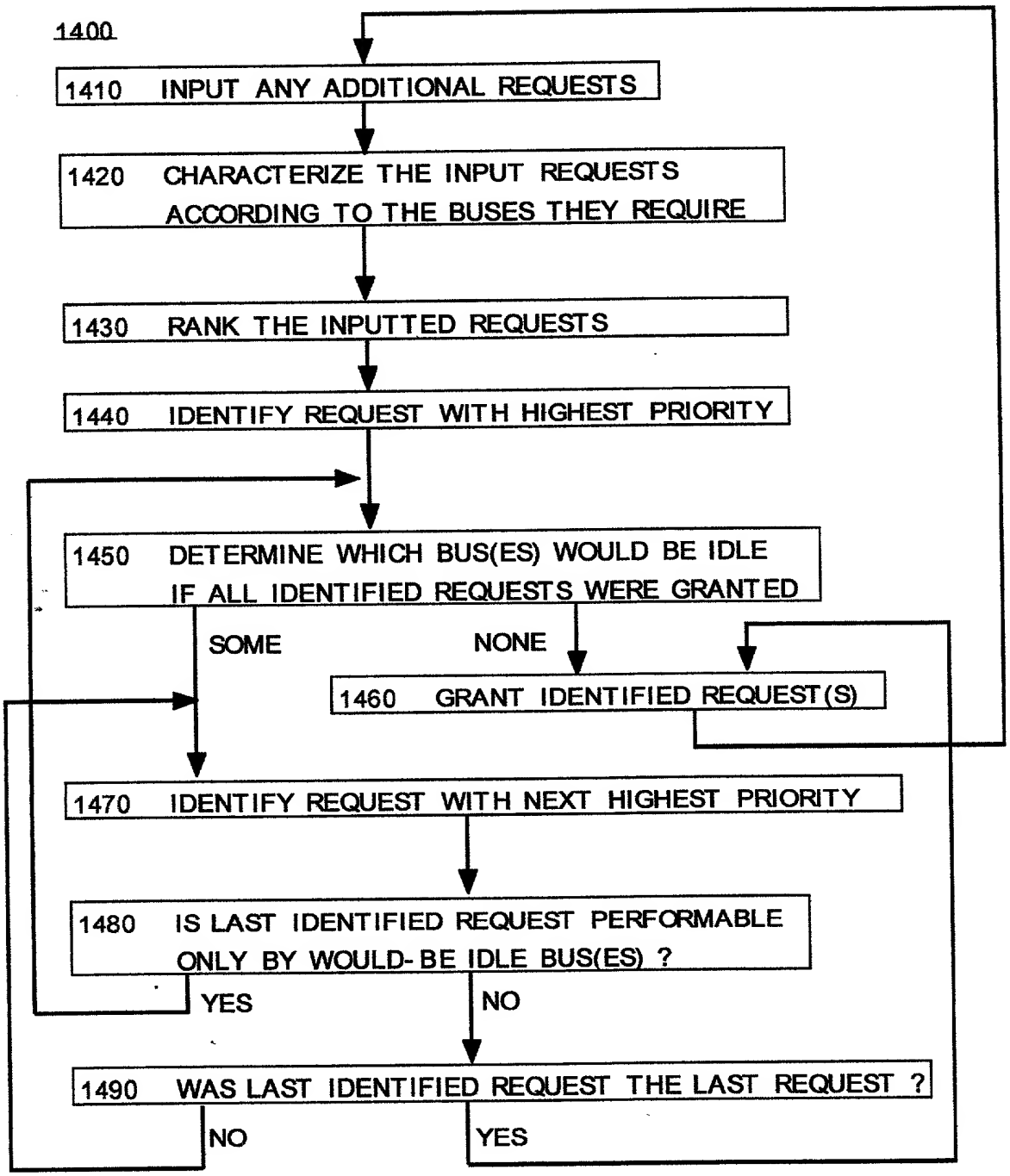
1400
1410 INPUT ANY ADDITIONAL REQUESTS
1420 CHARACTERIZE THE INPUT REQUESTS ACCORDING TO THE BUSES THEY REQUIRE
1430 RANK THE INPUTTED REQUESTS
1440 IDENTIFY REQUEST WITH HIGHEST PRIORITY
1450 DETERMINE WHICH BUS(ES) WOULD BE IDLE IF ALL IDENTIFIED REQUESTS WERE GRANTED
SOME
NONE
1460 GRANT IDENTIFIED REQUEST(S)
1470 IDENTIFY REQUEST WITH NEXT HIGHEST PRIORITY
1480 IS LAST IDENTIFIED REQUEST PERFORMABLE ONLY BY WOULD-BE IDLE BUS(ES) ?
YES
NO
1490 WAS LAST IDENTIFIED REQUEST THE LAST REQUEST ?
NO
YES

FIG.15

1500

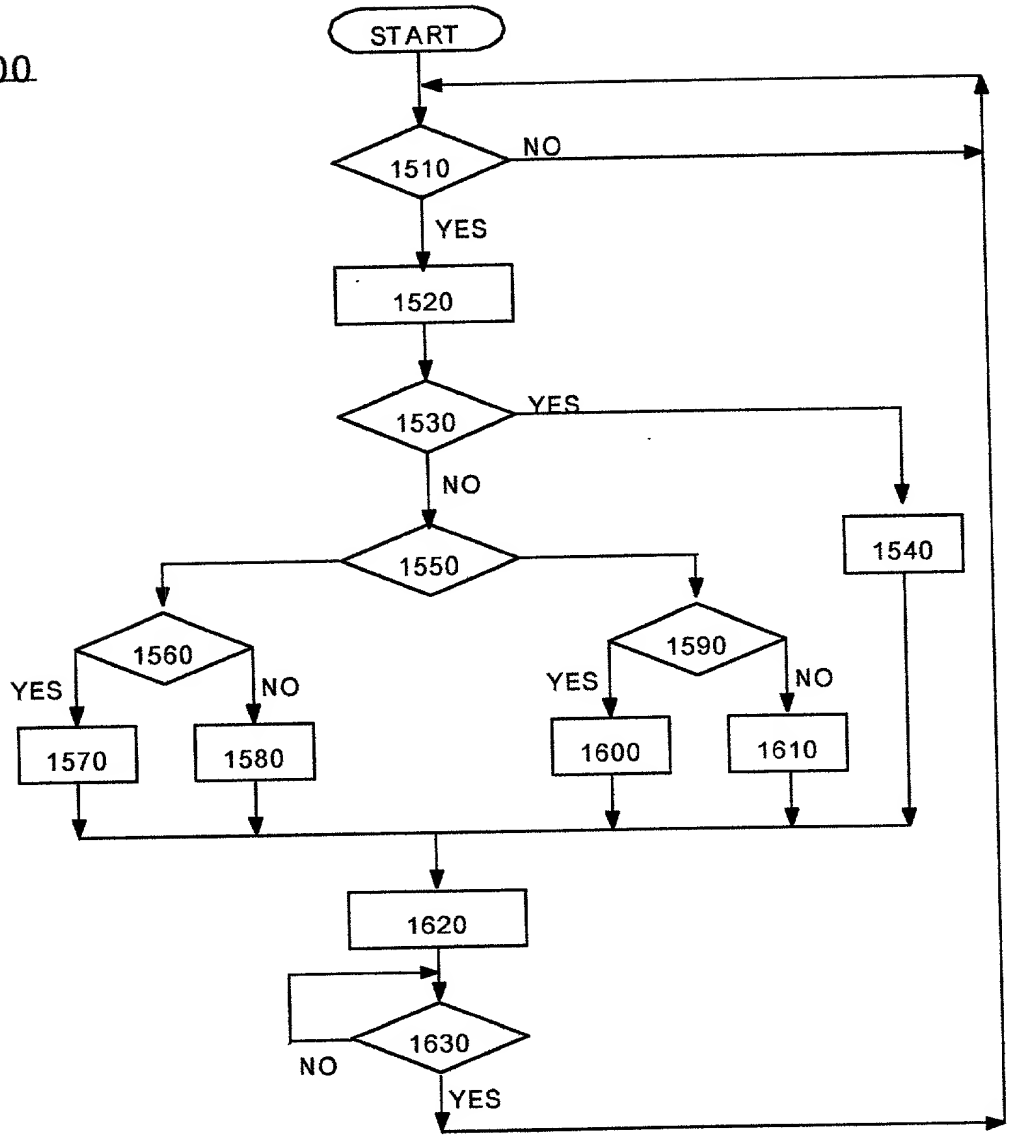
START
1510
NO
YES
1520
1530
YES
NO
1540
1550
1560
YES
NO
1570
1580
1590
YES
NO
1600
1610
1620
1630
NO
YES

FIG.16

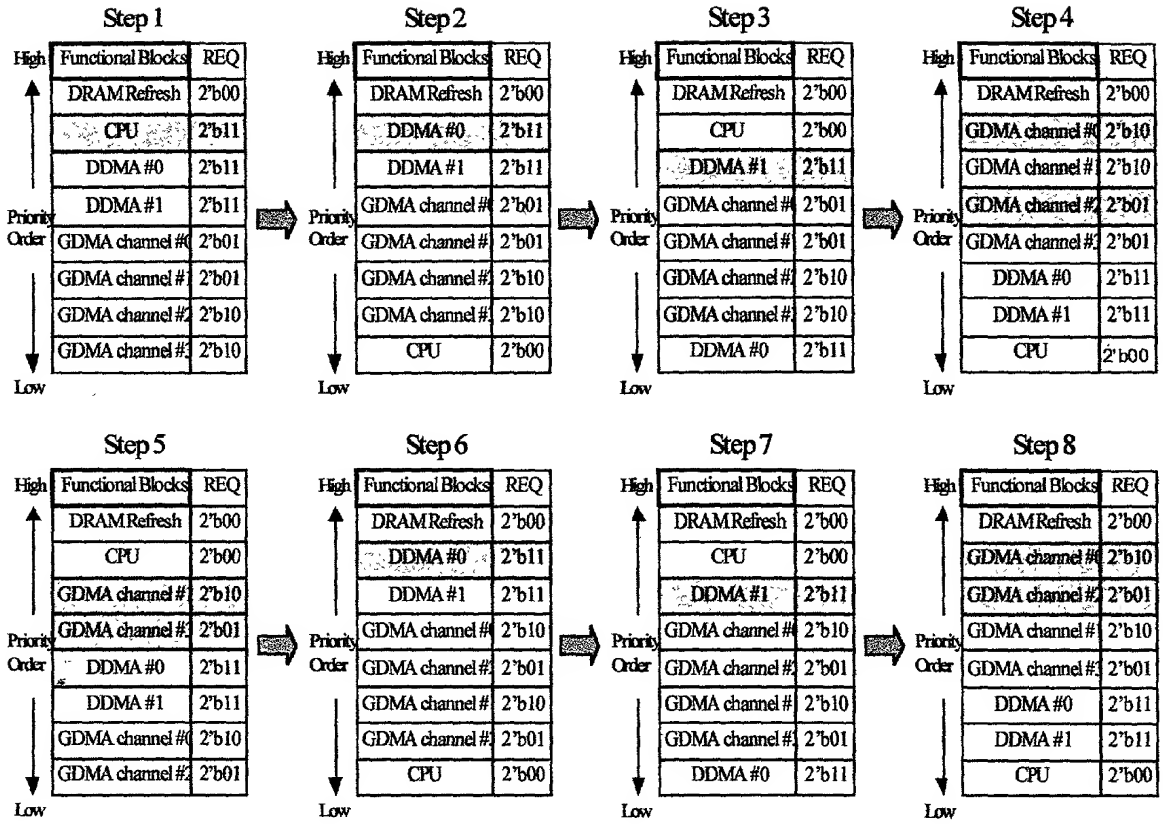

FIG.17

Item	Probability that element having bus ownership performs operation			Bus utilization
	Element of set EO	Element of set ES	Element of set SO	
Exclusive bus arbitration	$\frac{1}{n(A)}$	$\frac{1}{n(A)}$	$\frac{1}{n(A)}$	$\frac{n(EO)+2n(EO)+n(SO)}{2n(A)}$
Hierarchical bus arbitration	$\frac{n(ES)+2n(SO)}{2n(S)n(EO)}$	$\frac{1}{2n(S)}$	$\frac{1}{n(S)}$	$\frac{4n(SO)+3n(ES)}{4n(S)}$
Present invention	$\frac{n(EO)+n(SO)}{n(A)n(EO)}$	$\frac{1}{n(A)}$	$\frac{n(EO)+n(SO)}{n(A)n(SO)}$	1